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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,310	11/25/2003	Go Iwasaki	81788.0261	7084

26021 7590 01/30/2006

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 01/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/721,310	IWASAKI, GO	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 13-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1* is/are allowed.

6)☒ Claim(s) *2,5-10 and 13-16* is/are rejected.

7)☒ Claim(s) *3,4 and 17-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/19/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment filed on 11/16/2005 has been entered.

2. Claims 1-10, 13-19 are presented for examination.

Information Disclosure Statement

2. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 10/19/2005.

3. Information disclosed and list on PTO 1449 was considered.

Response to Arguments

3. Applicant's arguments with respect to claim1-19 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 2,5-7,8-10,13-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Gibbs et al. (U.S. Patent No. 6,384,621).

Regarding claims 2, Gibbs et al. disclose an output buffer circuit (Figure 1) comprising:

a plurality of unit circuits (Figure 1, 10, Figure 5a, 194) in each of which a plurality of pull-up transistors (Figure 1, 14) controlled by an input signal (Figure 1, IN) are connected in series between a high-potential power supply (Figgure1 , VCC) and common node nodes (Figure 1) , and a plurality pull-down transistors (Figure 1, 16) controlled by an input signal (Figure 1, IN) are connected in series between said common node nodes and a low-potential power supply (Figure 1, VSS);

an output terminal (Figure 1, OUT) connected to a common (Figure 1, 12) connecting point of said common nodes of said plurality of unit circuits (Figure 1) ; and

first resistors (Figure 1, 18) formed respectively between said common nodes of said plurality of unit circuits and said common connecting point (Figure 1).

Regarding claims 5-6, 7, Gibbs et al. disclose a third resistors (Figure 5b, 204, 208) formed respectively between the pull-up transistors (Figure 5b, 206) and common nodes and between the common nodes and pull-down transistors (Figure 5b, 210) in each of the plurality of unit circuits, and thirds transistors have the same resistance (Figure 5b), and wherein the first resistors formed between the common nodes and output terminal have the same resistance (Figure 1, RT).

Regarding claim 8, Gibbs et al. disclose wherein each of the pull-up and pull-down transistors is a MIS transistor (Figure 5b, 206, 210)

Regarding claim 9-10, Gibbs et al. disclose wherein said plurality of pull-up transistors have the same gate length and the same gate width, and said plurality of pull-down transistors have the same gate length and the same gate width (Column 7, lines 50-65), and wherein said resistor is selected from the group consisting of a metal film, composite metal film, metal cermet film, polysilicon film, diffusion layer, and transistor (Figure 5b).

Regarding claims 13-14, Gibbs et al. disclose an output buffer circuit (Figure 5a, 194) comprising:

a plurality of unit circuits (Figure b, 195) in each of which a pull-up transistor (Figure 5b, 206) controlled by a first input signal (Figure 5b, a signal coupled gate of 206) is connected between a high-potential power supply (Figure 5, VDD) and common node (Figure 5b), and a pull-down transistor (Figure 5b, 210) controlled by a second input signal (Figure 5b, a signal couple gate of 210) is connected between said common node and a low-potential power supply (Figure 5b, VSS) ;

an output terminal (Figure 5b, Figure 1, OUT) connected to a common connecting point of said common nodes of said plurality of unit circuits (Figure 5b) ; and

resistors (Figure 5b, 204, 208) formed respectively between said pull-up transistor and common node and between said common node and pull-down transistor in each of said unit circuits, and wherein the resistors formed respectively between the

pull-up and pull-down transistors and common node and between the common node and pull-down transistor have the same resistance (Figure 5b, Column 7, lines 50-65).

Regarding clams 15-16, Gibbs et al. disclose a semiconductor memory (Column 11, lines 8-17) comprising:

a plurality of memory cells((Column 11, lines 8-17) ;

a plurality of terminals including an output terminal (Figure 4, 108) ; and

an output buffer circuit (Figure 4, 120) positioned adjacent to said memory cell, said output buffer circuit comprising a plurality of unit circuits (Figure 5a, 194) in each of which a pull-up transistor (Figure 5b, 206) controlled by a first input signal (figure 5b, signal coupled to gate of 206) is connected between a high-potential power supply (Figure 5b, VDD) and common node (Figure 5b) and a pull-down transistor (Figure 5b, 210) controlled by a second input signal (Figure 5b, signal coupled to gate of 210) is connected between said common node and a low-potential power supply(Figure 5b, VSS) , and comprising first resistors (Figure 1, 18) connected respectively between said common nodes of said plurality of unit circuits and a common connecting point of said common nodes (Figure 1) , and wherein said first resistors are formed between said output buffer circuit and output terminal (Figure 1).

Allowable Subject Matter

6. Claim 1 is allowed.

Claim 1 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed

limitations. Gibbs et al. (U.S. Patent No. 6,384,621), and others, does not teach the claimed invention having an output buffer circuit including a plurality of unit circuits in each of which a pull-up transistor controlled by a first input signal is connected between a high-potential power supply and common node, and a first pull-down transistor controlled by a second input signal and a second pull-down transistor controlled by a third input signal are connected in series between said common node and a low-potential power supply as claim 1 disclosed.

Claims 3-4, 17-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3-4, 17-19 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Gibbs et al. (U.S. Patent No. 6,384,621), and others, does not teach the claimed invention having a second resistors formed respectively between said high-potential power supply and pull-up transistor and between said pull-down transistor and low-potential power supply in each of said plurality of unit circuits as claims 3-4 disclosed, and wherein if the number of said first resistors is an even number, said first resistors are symmetrically arranged with respect to a central line of said output buffer circuit and output terminal, and have the same value, the same size, and the same shape as claim 17 disclosed, and wherein said first resistors are formed on at least not less than one of three sides of said output terminal, which do not oppose said output buffer circuit as claims 18-19 disclosed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827

1/23/2005